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Date: OCTOBER 18, 2004

To: EXAMINER KIMBERLY D. NGUYEN
U.S. PATENT AND TRADEMARK OFFICE

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From: FRANK C. NICHOLAS
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Client/Matter No.: FR 000130 (7790/194)

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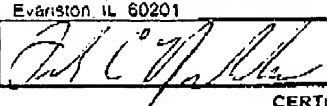
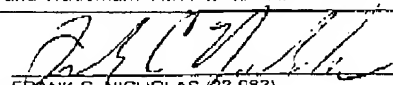
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	Application Number	10/015,985
	Filing Date	NOVEMBER 30, 2001
	First Named Inventor	YANNICK VINCENT
	Group Art Unit	2878
	Examiner	NGUYEN, KIMBERLY D

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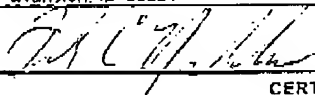
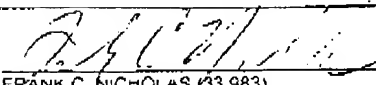
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	Application Number	10/015 965
	Filing Date	NOVEMBER 30, 2001
	First Named Inventor	YANNICK VINCENT
	Group Art Unit	2876
	Examiner	NGUYEN, KIMBERLY D

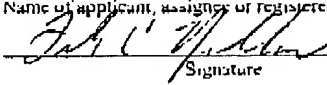
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PATENT
Case No. **FR 000130**
(7790/194)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of:)	
)	
YANNICK VINCENT)	
)	Examiner: Nguyen, Kimberly D.
Serial No.: 10/015,965)	
)	Group Art Unit: 2876
Filed: NOVEMBER 30, 2001)	
)	
For: DATA-PROCESSING SYSTEM)	

REPLY BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
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Dear Sir:

Appellant herewith respectfully presents a Reply Brief as follows:

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9. EVIDENCE APPENDIX.....	None
10. RELATED PROCEEDINGS APPENDIX.....	None

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1. REAL PARTY IN INTEREST

A statement of the real party in interest in contained in the Appeal Brief filed May 11, 2004.

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2. **RELATED APPEALS AND INTERFERENCES**

Appellant and the undersigned attorney are not aware of any other appeals or interferences which will directly affect or be directly affected by or having a bearing on the Board's decision in the pending appeal.

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3. STATUS OF CLAIMS

A statement of the status of the claims is in contained in the Appeal Brief filed
May 11, 2004.

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4. STATUS OF AMENDMENTS

A statement of the status of the amendments is in contained in the Appeal Brief
filed May 11, 2004.

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5. SUMMARY OF THE INVENTION

A statement of the summary of the invention is in contained in the Appeal Brief
filed May 11, 2004.

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6. GROUND OF REJECTION TO BE REVIEWED ON APPEAL

Pending claims 1, 3, 5, 7 and 9 stand finally rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,574,776 to *Chiang*.

Pending claims 2 and 6 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over *Chiang* in view of U.S. Patent Publication No. 2003/0004891 to *Van Rensberg*.

Pending claims 4 and 8 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over *Chiang* in view of U.S. Patent No. 5,978,822 to *Muwafi*.

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7. **ARGUMENT**

The Appellant respectfully asserts that a careful review of the Examiner's Answer reveals that Examiner Nguyen does not appreciate the scope of independent claims 1, 5 and 9, and does not understand the teachings of *Chiang*.

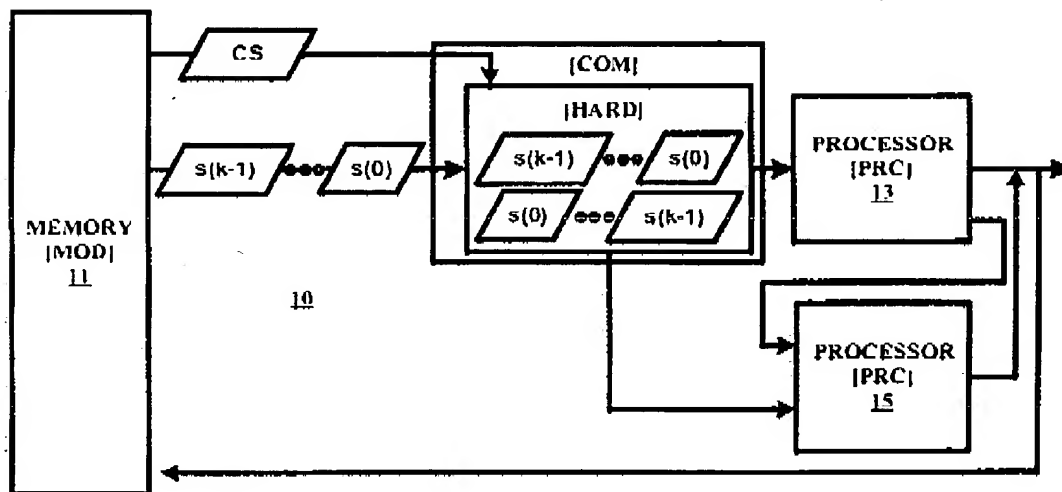
First, the scope of independent claims 1 and 5 encompasses "a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor", and "a hardware circuit [HARD] allowing an inversion of an order of bits of a word as a function of a value of the convention signal during a transfer of the word between said electronic module [MOD] and said microprocessor [PRC]", and the scope of independent claim 9 encompasses "a communication device [COM] for communicating a contention signal and a word to said hardware circuit [HARD] from one of a microprocessor [PRC] and an electronic module [MOD]" and "wherein said hardware circuit includes means for implementing one of a direct convention and an indirect convention of an order of bits of the word as a function of a value of the convention signal".

Second, *Chiang* teaches a modified procedure for using an array of data elements ($k=0, 1, \dots, 1117$) that are received separately at an EDC processor 13 (FIG. 1) and at an ECC P-parity processor 15 (FIG. 1), and processed in parallel in the two processors to compute an EDC error detection term and, simultaneously, to compute two ECC P-parity syndromes s_0 and s_1 . The procedure used at the EDC processor 13 computes the EDC

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term by receiving the sequence $\{s(k)\}$ of data elements ($k=0, 1, \dots, 1117$) in serial order and computing the EDC factor as the data elements are received. The procedure used in parallel at the ECC processor 15 computes components the two ECC syndromes as the data elements are received in serial order. See, Chiang at column 1, lines 33-45.

In view of the facts that (1) the scope of independent claims 1, 5 and 9 encompass a conditional inversion/convention of bits that is not performed during a transfer of bits to or from the processor, and (2) *Chiang* requires a serial reading of data elements $s(0) \dots s(k-1)$ from memory 11 to processors 13 and 15, *Chiang* would have to teach a device such as the device 10 illustrated below.



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Device 10 as shown includes a hardware circuit [HARD] that reads all of the data elements $s(0) \dots s(k-1)$ from memory [MOD] 11, and thereafter either serially transfers data elements $s(0) \dots s(k-1)$ to processors 13 and 15 as required by *Chiang* or inverts data elements to $s(k-1) \dots s(0)$ per a convention signal CS prior to serially transferring data elements $s(k-1) \dots s(0)$ to processors 13 and 15 as would be required by *Chiang* if *Chiang* taught an inversion of data elements $s(0) \dots s(k-1)$ prior to being serially transferred to processors 13 and 15.

Clearly, device 10 is within the scope of independent claims 1, 5 and 9, because any possible inversion of the data elements occurs during the transfer of the data elements from memory 11 to processor 13. Just as equally clear is the fact the *Chiang* teaches away from device 10 or any other device within the scope of independent claims 1, 5 and 9 by teaching a EDC error detection and an ECC P-parity syndromes s_0 and s_1 generation that are based on a serial transfer of data elements $s(0) \dots s(k-1)$ from memory 11 to processors 13 and 15 that must not be inverted as the data elements $s(0) \dots s(k-1)$ are serially transferred from memory 11 to processors 13 and 15.

To support his untenable rejection of independent claims 1, 5 and 9 as being anticipated by *Chiang*, Examiner Nguyen improperly asserts that an EDC inverter (FIG. 7) within processor 13, which "conditionally" inverts a block of data elements "during" the serial transfer of the block of the data elements from memory 11 to processor 13, anticipates the hardware circuit [HARD] as recited in independent claims 1, 5 and 9. However, a proper understanding of *Chiang* reveals the fact that the EDC inverter within processor 13 "unconditionally" inverts a block of data elements "after", not during, the serial transfer of the block of the data elements from memory 11 to processor 13, and therefore does not anticipate the hardware circuit [HARD] as recited in independent claims 1, 5 and 9.

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Furthermore, in the Appeal Brief, the Appellant provided a SUMMARY OF THE INVENTION as mandated by the regulations, and provided an ARGUMENTS as mandated the regulations. A careful review of the Appeal Brief reveals the fact that, in supporting the arguments as to why claims 1-9 are patentable over *Chiang*, the Appellant DID NOT recite any portion of the SUMMARY OF THE INVENTION in the ARGUMENTS as improperly and inappropriately asserted by Examiner Nguyen in section (II) 4. of the Examiner's Answer.

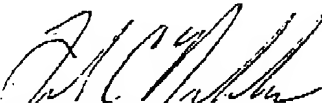
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Respectfully submitted,
Yannick Vincent

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October 18, 2004

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CLAIMS APPENDIX

1. A data-processing system, comprising:
 - a microprocessor [PRC];
 - a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor; and
 - a hardware circuit [HARD] allowing an inversion of an order of bits of a word as a function of a value of the convention signal during a transfer of the word between said electronic module [MOD] and said microprocessor [PRC].
2. The data-processing system as claimed in claim 1, wherein said electronic module [MOD] is a Subscriber Identity Module card.
3. The data-processing system as claimed in claim 1, wherein said hardware circuit [HARD] allows inversion of the value of the bits of the word as a function of the value of the convention signal.
4. The data-processing system as claimed in claim 1, wherein said hardware circuit [HARD] includes:
 - a switch [SWHMP, SWHPM];
 - a right shift register [RXMP, RYPM] electrically connected to said switch; and
 - a left shift register [RYMP, RXPM] electrically connected to said switch.

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5. A terminal, comprising:
a microprocessor [PRC];
a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor; and
a hardware circuit [HARD] allowing an inversion of an order of bits of a word as a function of a value of the convention signal during a transfer of the word between said electronic module [MOD] and said microprocessor [PRC].
6. The terminal as claimed in claim 5, wherein said electronic module [MOD] is a Subscriber Identity Module card.
7. The terminal as claimed in claim 5, wherein said hardware circuit [HARD] allows inversion of the value of the bits of the word as a function of the value of the convention signal.
8. The terminals as claimed in claim 5, wherein said hardware circuit [HARD] includes:
a switch [SWHMP, SWHPM];
a right shift register [RXMP, RYPM] electrically connected to said switch; and
a left shift register [RYMP, RXPM] electrically connected to said switch.

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9. A data-processing system, comprising:

a hardware circuit [HARD];

a communication device [COM] for communicating a contention signal and a word to said hardware circuit [HARD] from one of a microprocessor [PRC] and an electronic module [MOD]; and

wherein said hardware circuit includes means for implementing one of a direct convention and an indirect convention of an order of bits of the word as a function of a value of the contention signal.

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EVIDENCE APPENDIX

None.

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RELATED PROCEEDINGS APPENDIX

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